Original

6/12/03

REMARKS

Claims 1-20 are pending. Applicants respectfully traverse, request reconsideration and withdrawal of the rejections for the following reasons.

I. Summary of the Examiner's Objections/Rejections

Claims 1-10 and 12-19 are rejected under 35 U.S.C. §103(a) over U.S. Patent Number 6,446,193 to Alidina et al. "Alidina" in view of U.S. Patent No. 5,896,517 to Wilson. Claims 11 and 20 are rejected under 35 U.S.C. §103(a) over Alidina in view of Wilson and in further view of U.S. Patent Number 5,673,377 to Berkaloff. Claim 16 is objected to due to an informality.

II. Applicant's Response to the Examiner's Rejections

The Applicants traverse the aforementioned claim rejections for at least the reasons set forth in greater detail below.

A. Objection to Claim 16.

The Applicants' attorney thanks the Examiner for the suggestion; however, the replacement language appears identical to the language to replace. A clarification is requested.

B. 35 U.S.C. §103(a); Claims 1-10 and 12-19.

According to the Office Action, claims 1-10 and 12-19 are rejected under 35 U.S.C. §103(a) over U.S. Patent Number 6,446,193 to Alidina et al. "Alidina" in view of U.S. Patent No. 5,896,517 to Wilson.

Alidina is directed to reducing instruction cycles in a digital signal processor by processing two different register parts in a single processor cycle instead of two. (Alidina, Col. 2, lines 42-56).

Wilson is directed to a method for improving the performance of a computer system by adding instructions at the program writing stage, by the programmer or by software tools such as

a compiler, to prefetch data from main memory in order to avoid the overhead of multi-threaded process swapping because of blocking, such as a cache miss. (Wilson, Col. 3, lines 14-28). The overhead of multi-threaded process swapping (such as needing data from a disk due to a cache miss) can be quite expensive since there may be many registers to save and restore. (Wilson, Col. 2, lines 34-65). Because of the high overhead costs, and because such process-swapping is always unexpected, "It is desirable to avoid the overhead costs of process-swapping," i.e., the multi-threaded processor scheme. (Wilson, Col. 2, line 66- Col. 3 line 3).

NEITHER ALIDINA NOR WILSON TEACHES AT LEAST "WHEREIN A SELECTED ACCUMULATION REGISTER THAT CORRESPONDS TO THE SELECTED THREAD STORES THE FIRST OPERATION RESULT CORRESPONDING TO THE SELECTED THREAD"

The Office Action fails to establish a *prima facie* case of obviousness because the Office Action fails to show how each and every element in the claims is taught by the references. To establish a *prima facie* case of obviousness, each and every element arranged, as required by the claims, must be taught or suggested in the prior art. MPEP 2143.03.

Firstly, the Office Action acknowledges that Alidina does not teach, "wherein a selected accumulation register that corresponds to the selected thread stores the first operation result corresponding to the selected thread." Further, Alidina is directed to processing two different register parts in a single processor cycle for speech coding and, as a result, is directed to a problem different than the claims. Wilson not only fails to teach, among other things, a multi-threaded system as claimed. Wilson teaches, "it is desirable to avoid the overhead costs of processing swapping," i.e., multi-threaded context switching, because multi-threaded switching can be quite expensive since there may be many registers to save and restore. Secondly, Wilson as cited fails to teach, "wherein a selected accumulation register that corresponds to the selected thread stores the first operation result corresponding to the selected thread" because, in contrast

to the claims, Wilson teaches away from multi-threaded processing. Further, Wilson teaches away from storing a thread in an accumulation register because not only does Wilson teach away from multi-threaded processing, Wilson teaches "multi-threaded context switching can be quite expensive since there may be many registers to save and restore." Therefore, the combination of Alidina in view of Wilson as cited fails to teach "wherein a selected accumulation register that corresponds to the selected thread stores the first operation result corresponding to the selected thread" as arranged in the claims. Consequently, the Office Action fails to establish a *prima facie* case of obviousness.

Thirdly, there is no motivation to combine Alidina with Wilson because Wilson teaches against the claims since, as previously stated, Wilson teaches avoiding multi-threaded context switching to avoid the expense of "many registers to save and restore." (Wilson, Col. 2, line 66-Col. 3 line 3). The very portion of Wilson cited in the Office Action to provide motivation to combine Alidina with the teachings of Wilson actually teaches against the claims. As previously stated, Wilson teaches "with a multi-threaded processor, context switching can be quite expensive since there may be many registers to save and restore" and, therefore, multi-threaded processing is avoided. Consequently, the Office Action fails to establish a *prima facie* case of obviousness.

Fourthly, to the extent Alidina and Wilson may be combined, such a combination would teach reducing instruction cycles in a digital signal processor by processing two different register parts in a single processor cycle, instead of two, by adding instructions at the program writing stage, by the programmer or by software tools, such as a compiler, to prefetch data from main memory in order to avoid the overhead of multi-threaded process swapping. As a result, the combination of Alidina and Wilson is directed to a different problem than the claims. Therefore,

the combination of Alidina in view of Wilson as cited teaches away from the claims and fails to teach each and every element as arranged in the claims. Consequently, the Office Action fails to establish a *prima facie* case of obviousness.

THE MODIFICATION OF ALIDINA AS SUGGESTED BY WILSON WOULD CHANGE THE PRINCIPLE OF OPERATION OF THE CLAIMED INVENTION AND THEREFORE THE OFFICE ACTION FAILS TO PROVIDE ANY MOTIVATION TO COMBINE THE REFERENCES

Fifthly, the modification of Alidina, in view of the cited suggestion of Wilson, would change the principle of operation of the claimed invention because the modification suggested by Wilson, as previously stated, rather than teaching multi-threaded context switching, teaches "it is desirable to avoid the overhead costs of process-swapping." Instead of multi-threaded processing as claimed, Wilson teaches coding at the program writing stage to prefetch data. Further, the proposed combination teaches multi-threaded context switching can be quite expensive since there may be many registers to save and restore. Therefore, the modification suggested by Wilson would change the principle of operation of the claimed invention because Wilson (1) teaches coding at the program writing stage to prefetch data (2) teaches against multi-threaded context switching, and (3) teaches against saving and restoring registers. Consequently, for at least these reasons, there is no motivation to combine the references and, therefore, the Office Action fails to establish a *prima facie* case of obviousness.

/ / /

/ / /

/ / /

/ / /

/ / /

NEITHER ALIDINA NOR WILSON TEACHES AT LEAST "A FIRST OPERATION UNIT OPERABLY COUPLED TO RECEIVE A FIRST OPERAND AND A SECOND OPERAND CORRESPONDING TO AN OPERATION CODE ISSUED BY A SELECTED THREAD OF THE PLURALITY OF THREADS, WHEREIN THE OPERATION UNIT COMBINES THE FIRST AND SECOND OPERANDS TO PRODUCE A FIRST OPERATION RESULT CORRESPONDING TO THE SELECTED THREAD"

Sixthly, the Office Action cites Alidina (Alidina, Abstract, lines 1-4; column 2, lines 46-48; columns 4-5, lines 26-7; and Figure 3) for teaching "a first operation unit operably coupled to receive a first operand and a second operand corresponding to an operation code issued by a selected thread of the plurality of threads." However, this general reference to over 70 lines in a reference without showing equivalent claim elements does not make apparent nor explain with specificity how each claim is rejected. MPEP 706, CFR 1.104(c)(2). For example, Applicants are unable to find any reference in Alidina as cited, "corresponding to an operation code issued by a selected thread of the plurality of threads" as claimed. As previously stated, Applicants cannot find where Alidina teaches multi-threaded processing. Further, Wilson teaches against a multi-threaded processor since Wilson teaches, "it is desirable to avoid the overhead costs of processing swapping" and multi-threaded context switching can be quite expensive since there may be many registers to save and restore. Consequently, among other things, the combination of Alidina in view of Wilson as cited fails to teach "a first operation unit operably coupled to receive a first operand and a second operand corresponding to an operation code issued by a selected thread of the plurality of threads." Therefore, the combination of Alidina in view of Wilson as cited fails to teach each and every element as arranged in the claims. Consequently, the Office Action fails to establish a *prima facie* case of obviousness.

Seventhly, the Office Action fails to indicate and Applicants are unable to find any reference to where Alidina or Wilson as cited teaches, "wherein the operation unit combines the

first and second operands to produce a first operation result corresponding to the selected thread." The Office Action acknowledges that Alidina fails to teach, "wherein a selected accumulation register that corresponds to the selected thread stores the first operation result corresponding to the selected thread." As previously stated, Wilson teaches against multithread processing. Consequently, the combination of Alidina and Wilson teaches against "wherein the operation unit combines the first and second operands to produce a first operation result corresponding to the selected thread." If the Examiner maintains this rejection, Applicants respectfully request a recitation in Alidina and Wilson of each and every element arranged as claimed.

NEITHER ALIDINA NOR WILSON TEACHES AT LEAST "A SELECTION BLOCK OPERABLY COUPLED TO THE PLURALITY OF ACCUMULATION REGISTERS AND THE FIRST OPERATION UNIT, WHEREIN THE SELECTION BLOCK SELECTS THE SECOND OPERAND PROVIDED TO THE FIRST OPERATION UNIT FROM A SET OF POTENTIAL OPERANDS, WHEREIN THE SET OF POTENTIAL OPERANDS INCLUDES CONTENTS OF EACH ACCUMULATION REGISTER OF THE PLURALITY OF ACCUMULATION REGISTERS "

Eighthly, the combination of Alidina and Wilson fail to teach "a selection block operably coupled to the plurality of accumulation registers and the first operation unit, wherein the selection block selects the second operand provided to the first operation unit from a set of potential operands, wherein the set of potential operands includes contents of each accumulation register of the plurality of accumulation registers." (Alidina, Col. 4, lines 57-59). Alidina, as cited in the Office Action, asserts that the SMUX in Alidina is the claimed selection block. However, as shown in Figure 3, Alidina does not provide a path from the control registers via the SMUX to the first operation unit (no equivalent element in Alidina identified in the Office Action), but rather the XYFB couples SMUX to the register X(32). In Alidina "the eight accumulators are controlled according to modes defined by preselected mode bits provided by

control registers auc0 and auc1 to selectively provide feedback along a feedback path XYFBK to the x-y multiplier registers x(32) and y(32)." (Alidina Col 5. lines 13-17). If the rejection is maintained, and the registers x(32) in Alidina are equated to the first operation unit, then Alidina fails to teach at least "wherein the operation unit combines the first and second operands to produce a first operation result corresponding to the selected thread" as claimed. Therefore, Alidina does not teach "wherein the selection block selects the second operand provided to the first operation unit from a set of potential operands, wherein the set of potential operands includes contents of each accumulation register of the plurality of accumulation registers." Therefore, the combination of Alidina in view of Wilson, as cited, fails to teach each and every element as arranged in the claims. Consequently, the Office Action fails to establish a *prima facie* case of obviousness.

C. 35 U.S.C. §103(a): Claims 11 and 20.

Claims 11 and 20 are rejected under 35 U.S.C. §103(a) over Alidina in view of Wilson and, in further view, of U.S. Patent Number 5,673,377 to Berkaloff. The Office Action acknowledges that Alidina does not teach wherein the first register section accumulates diffuse color information corresponding to graphics primitives, and wherein the second register section accumulates specular color information corresponding to the graphics and primitives. Further, the motivation provided in the Office Action to combine the references "because it is needed in the calculations to create effective images" provides no basis for the meaning of "effective images" and further uses circular reasoning and therefore fails to establish motivation to combine the references. Claims 11 and 20 add additional novel and nonobvious subject matter and are also allowable at least for the above reasons and as depending from an allowable base claim.

As to claim 2, the Office Action cites Alidina as teaching a control block as claimed. However, this portion describes bus-accessible control registers rather than "a control block

operably coupled to the selection block and the plurality of accumulation registers, wherein the control block receives information based on the operation code and generates control information provided to the plurality of accumulation registers and the selection block, wherein the control information provided to the plurality of accumulation registers causes the selected accumulation register to store the result corresponding to the selected thread when the operation code corresponds to an accumulate operation." The Office Action fails to show how Alidina teaches that the bus-accessible control registers are equivalent to the control block as claimed and, therefore, fails to establish a *prima facie* case of obviousness. Applicants at least reassert that the references do not teach each and every element as arranged in the claims with respect to claim 1. Claim 2 adds additional novel and nonobvious subject matter for at least these reasons and is also allowable at least as depending from an allowable base claim.

As to claims 3, 4, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 18, and 19, Applicants at least reassert the above reasons. Each claim adds additional novel and nonobvious subject matter and are at least as depending from an allowable base claim. Further, the combined references do not teach each and every element as arranged in the claims.

As to claims 7 and 17, the cited portion of Wilson, rather than teaching an arbitration module as asserted in the Office Action, teaches against arbitration in a multi-threaded processor since Wilson teaches against multi-threaded processing as previously stated. Accordingly, the assertion that it is inherent that there must be a unit as claimed is improper. Accordingly, a supporting reference is respectfully requested if the rejection is maintained. Applicants also at least reassert that the references do not teach each and every element as arranged in the claims with respect to claim 1. Claims 7 and 17 add additional novel and nonobvious subject matter and are also allowable at least as depending from an allowable base claim.

Applicant respectfully submits that the claims are in condition for allowance and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

By _____
Themi Anagnos, Reg. No. 47,388

Date: June 12, 2003

Vedder, Price, Kaufman & Kammholz
222 North LaSalle Street
Chicago, Illinois 60601
PHONE: (312) 609-7970
FAX: (312) 609-5005